In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1-13. (Canceled)

14. (Previously presented) A master-slave electronic fuse for selectively configuring a circuit, comprising:

a master fuse having a master latch and a nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and the master latch, said master latch comprising cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters, said nonvolatile memory element comprising a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value; and

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node, said predetermined state of the master latch to which the slave latch is configured to latch being one of two states each corresponding to a different configuration of the circuit such that said fuse is operative to configure the circuit in accordance with a value stored in the nonvolatile memory element and following application of the reset signal,

wherein the predetermined state of said master latch is affected by a memory value to which the nonvolatile memory element is programmed, and

wherein the master latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.

15. (Canceled)

16. (Previously presented) The master-slave electronic fuse of Claim 14, wherein said master latch comprises cross-coupled inverters.

17. (Canceled)

18. (Previously presented) The master-slave electronic fuse of Claim 14, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

19. (Previously presented) The master-slave electronic fuse of Claim 14, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

20. (Previously presented) The master-slave electronic fuse of Claim 14, wherein said floating-gate transistor is MOS device.

21. (Original) The master-slave electronic fuse of Claim 14, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

22. (Previously presented) The master-slave electronic fuse of Claim 14, wherein the amount of charge on the floating gate is changeable using any one or more of Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, hot-hole injection, and ultraviolet radiation.

23-26. (Canceled)

27. (Previously presented) The master-slave electronic fuse of Claim 14, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

28. (Original) The master-slave electronic fuse of Claim 14, further comprising a capacitive element coupled to an output of the master latch.

29. (Canceled)

30. (Previously presented) The master-slave electronic fuse of claim 14, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

31-32. (Canceled)

33. (Previously presented) A master-slave electronic fuse for configuring a circuit comprising:

a master fuse having a master latch with a first output capacitively coupled to a first source of a fixed voltage and a second output capacitively coupled to a second source of a fixed voltage which is the same as first source, the master fuse further having a first nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and first node of the master latch, and a second nonvolatile memory element coupled between the reset node and a second node of the master latch, said first nonvolatile memory element comprising a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value, and said second nonvolatile memory element comprising a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value;

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, the predetermined state of the master latch being affected by a first memory value associated with the first nonvolatile

memory element and is affected by a second memory value associated with the second nonvolatile memory element, and wherein the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node, and wherein the first state to which the master latch is configured to settle is operative to configure the circuit to a corresponding first configuration and the second state to which the master latch is configured to settle is operative to configure the circuit to a corresponding second configuration.

34-38. (Canceled)

39. (Previously presented) The master-slave electronic fuse of Claim 33, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

40. (Original) The master-slave electronic fuse of Claim 39, wherein said second nonvolatile memory element further comprises a second capacitor having a first plate in common with the second floating gate.

41. (Original) The master-slave electronic fuse of Claim 33, wherein said first and second nonvolatile memory elements comprise nonvolatile memory elements manufactured in a MOS fabrication process.

42. (Previously presented) The master-slave electronic fuse of Claim 33, wherein at least one of said first and second floating-gate transistors are MOS devices.

43. (Original) The master-slave electronic fuse of Claim 33, wherein at least one of said first and second nonvolatile memory elements use a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

44. (Previously presented) The master-slave electronic fuse of Claim 33, wherein the amount of charge on at least one of the first and second floating gates is changeable using any one or

more of Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, hot-hole injection, and ultraviolet radiation.

45-48. (Canceled)

49. (Original) The master-slave electronic fuse of Claim 41, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

50. (Original) The master-slave electronic fuse of Claim 49, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

51-53. (Canceled)

54. (Previously presented) The master-slave electronic fuse of claim 33, wherein the master latch is predisposed to settle into one of said first and second states in response to said first and second memory values.

55. (Original) The master-slave electronic fuse of claim 54, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

56-73. (Canceled)

74. (Previously presented) A master-slave electronic fuse for selectively configuring a circuit, comprising:

a master fuse having a master latch and a nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and the master latch, said master latch comprising cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters, said nonvolatile memory

element comprising a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value; and

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node, said predetermined state of the master latch to which the slave latch is configured to latch being one of two states each corresponding to a different configuration of the circuit such that said fuse is operative to configure the circuit in accordance with a value stored in the nonvolatile memory element and following application of the reset signal,

wherein the predetermined state of said master latch is affected by a memory value to which the nonvolatile memory element is programmed, and

wherein the master latch is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.

75. (Previously presented) The master-slave electronic fuse of Claim 74, wherein said master latch comprises cross-coupled inverters.

76. (Previously presented) The master-slave electronic fuse of Claim 74, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

77. (Previously presented) The master-slave electronic fuse of Claim 74, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

78. (Previously presented) The master-slave electronic fuse of Claim 74, wherein said floating-gate transistor is MOS device.

79. (Previously presented) The master-slave electronic fuse of Claim 74, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

80. (Previously presented) The master-slave electronic fuse of Claim 74, wherein the amount of charge on the floating gate is changeable using any one or more of Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, hot-hole injection, and ultraviolet radiation.

81. (Previously presented) The master-slave electronic fuse of Claim 74, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

82. (Previously presented) The master-slave electronic fuse of Claim 74, further comprising a capacitive element coupled to an output of the master latch.

83. (Previously presented) The master-slave electronic fuse of Claim 74, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

84. (Previously presented) A master-slave electronic fuse for configuring a circuit comprising:

a master fuse having a master latch comprising cross-coupled inverters, wherein a first one of the cross-coupled inverters has at least one transistor with a gate width-to-length ratio that is larger than a gate width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters, the master fuse further having a first nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and first node of the master latch, and a second nonvolatile memory element coupled between the reset node and a second node of the master latch, said first nonvolatile memory element comprising a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining

said first memory value, and said second nonvolatile memory element comprising a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value;

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node and is predisposed to settle into one of said first and second states in response to said first and second memory values, the predetermined state of the master latch being affected by a first memory value associated with the first nonvolatile memory element and is affected by a second memory value associated with the second nonvolatile memory element, and wherein the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node, and wherein the first state to which the master latch is configured to settle is operative to configure the circuit to a corresponding first configuration and the second state to which the master latch is configured to settle is operative to configure the circuit to a corresponding second configuration.

85-86. (Canceled)

87. (Previously presented) The master-slave electronic fuse of Claim 84, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

88. (Previously presented) The master-slave electronic fuse of Claim 87, wherein said second nonvolatile memory element further comprises a second capacitor having a first plate in common with the second floating gate.

89. (Previously presented) The master-slave electronic fuse of Claim 84, wherein said first and second nonvolatile memory elements comprise nonvolatile memory elements manufactured in a MOS fabrication process.

90. (Previously presented) The master-slave electronic fuse of Claim 84, wherein at least one of said first and second floating-gate transistors are MOS devices.

91. (Previously presented) The master-slave electronic fuse of Claim 84, wherein at least one of said first and second nonvolatile memory elements use a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

92. (Previously presented) The master-slave electronic fuse of Claim 84, wherein the amount of charge on at least one of the first and second floating gates is changeable using any one or more of Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, hot-hole injection, and ultraviolet radiation.

93. (Previously presented) The master-slave electronic fuse of Claim 89, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

94. (Previously presented) The master-slave electronic fuse of Claim 93, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

95. (Previously presented) The master-slave electronic fuse of Claim 84, wherein a first output of said master latch is capacitively coupled to a first source of a fixed voltage.

96. (Previously presented) The master-slave electronic fuse of Claim 95, wherein a second output of said master latches is capacitively coupled to a second source of a fixed voltage.

97. (Previously presented) The master-slave electronic fuse of Claim 96, wherein said first source of a fixed voltage and said second source of a fixed voltage are the same.

98. (Previously presented) The master-slave electronic fuse of Claim 84, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

99. (Previously presented) A master-slave electronic fuse for configuring a circuit comprising:

a master fuse having a master latch comprising cross-coupled inverters, wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters, the master fuse further having a first nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and first node of the master latch, and a second nonvolatile memory element coupled between the reset node and a second node of the master latch, said first nonvolatile memory element comprising a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value, and said second nonvolatile memory element comprising a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value;

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node and is predisposed to settle into one of said first and second states in response to said first and second memory values, the predetermined state of the master latch being affected by a first memory value associated with the first nonvolatile memory element and is affected by a second memory value associated with the second nonvolatile memory element, and wherein the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node, and wherein the first state to which the master latch is configured to settle is operative to configure the circuit to a corresponding first configuration and the second state to which the master latch is configured to settle is operative to configure the circuit to a corresponding second configuration.

100-101. (Canceled)

102. (Previously presented) The master-slave electronic fuse of Claim 99, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

103. (Previously presented) The master-slave electronic fuse of Claim 102, wherein said second nonvolatile memory element further comprises a second capacitor having a first plate in common with the second floating gate.

104. (Previously presented) The master-slave electronic fuse of Claim 99, wherein said first and second nonvolatile memory elements comprise nonvolatile memory elements manufactured in a MOS fabrication process.

105. (Previously presented) The master-slave electronic fuse of Claim 99, wherein at least one of said first and second floating-gate transistors are MOS devices.

106. (Previously presented) The master-slave electronic fuse of Claim 99, wherein at least one of said first and second nonvolatile memory elements use a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

107. (Previously presented) The master-slave electronic fuse of Claim 99, wherein the amount of charge on at least one of the first and second floating gates is changeable using any one or more of Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, hot-hole injection, and ultraviolet radiation.

108. (Previously presented) The master-slave electronic fuse of Claim 104, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

109. (Previously presented) The master-slave electronic fuse of Claim 108, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

110. (Previously presented) The master-slave electronic fuse of Claim 99, wherein a first output of said master latches is capacitively coupled to a first source of a fixed voltage.

111. (Previously presented) The master-slave electronic fuse of Claim 110, wherein a second output of said master latches is capacitively coupled to a second source of a fixed voltage.

112. (Previously presented) The master-slave electronic fuse of Claim 111, wherein said first source of a fixed voltage and said second source of a fixed voltage are the same.

113. (Previously presented) The master-slave electronic fuse of Claim 99, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.